Kratik Jain

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B.Tech - Electronics and Communication Engineering

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Education

Degree/Certificate	Institute/Board	CGPA/Percentage	Year
B.Tech. ECE	Sardar Vallabhbhai National Institute of Technology,Surat	7.55	2025
Senior Secondary	MPBSE Board	94.8%	2021
Secondary	CBSE Board	93.8%	2019

Projects

•RV32IM Pipelined RISC-V Processor Core Dec. 2025

A 5-Stage Pipelined 32-bit RISC-V Processor with Hardware M-Extension & Automated Verification **Github**

– Designed and implemented a **synthesizable 5-stage in-order RV32IM RISC-V microarchitecture** in **Verilog**, supporting **47+ instructions** across arithmetic, control-flow, memory, and **M-extension operations**.

– Architected a **scoreboard-based issue unit** with **multi-stage dependency tracking** and **3-path operand forwarding (E1/E2/WB bypass network)** to resolve **RAW hazards** and minimize pipeline stalls.

– Developed a **2-stage pipelined hardware multiplier** (MUL/MULH/MULHSU/MULHU) and an **iterative non-restoring divider** (DIV/DIVU/REM/REMU) with **out-of-pipeline completion**, **handshake-based control**, and **dynamic stall management**.

– Designed a **synchronous Load/Store Unit** with **byte-enable generation**, **sub-word alignment detection**, **sign/zero extension logic**, and a **request-tracking FIFO**; integrated **BRAM-based instruction and data memories** optimized for FPGA resource utilization.

– Built an **automated regression and verification flow** using **Python, TCL, and Shell scripting** to assemble, convert, and batch-simulate RISC-V programs in **Vivado**; achieved **timing closure** and validated on **Basys-3 FPGA** with **ILA-based on-chip debugging**.

•High-Performance Cache Architecture Design Mar. 2025

Optimized memory access with advanced cache implementation.

– Designed and implemented a **4-way set-associative data cache** and **2-way set-associative instruction cache** with **LRU replacement policy**, valid/dirty bit management, and tag comparison logic.

– Developed a **cache miss handling FSM** supporting **dirty line write-back** and **memory block refill**, ensuring correct and efficient memory hierarchy operation.

– Integrated **parameterized memory models** and built comprehensive **self-checking testbenches** to validate hit, miss, write-back, and eviction scenarios.

– Automated regression using **Vivado xsim (batch mode)** with **TCL scripting**, generated **VCD waveforms**, and performed detailed timing/debug analysis using **GTKWave**.

– Verified functional correctness across multiple **cache configurations** (varying sizes and associativity), replacement policies, and memory transaction patterns.

Technical Skills

- **Programming Languages**: Verilog,C,C++,Python
- **EDA & Tools**: Vivado,Cadence,Matlab,keil Uvision,GTKWave,Git/Github,Visual Studio Code
- **Operating Systems**: Linux, Windows
- **CS Fundamentals**: Machine Learning,Deep Learning,Data Structures and Algorithms,OOPS

Experience

•NSE Clearing Limited *Aug 2025 - Present*

System Analyst Mumbai, India

– Developed backend services using **Spring Boot** and **gRPC**, optimizing inter-service communication and latency.

– Built cross-platform desktop tooling using **Rust (Tauri)** and integrated **HTTP/2-based communication**.

•Keysight Technologies *March 2025 - June 2025* ***Certificate***

Intern Tech I Gurugram,India

– Migrated enterprise configuration logic from **Oracle CPQ** to **Logik CPQ** and Salesforce, implementing rule engines and backend integrations.

– Improved quoting performance by **40%** and reduced maintenance overhead by **50–80%** through optimized business logic restructuring.

Key courses taken

- **Electronics**: VLSI Design,Processor Architecture,Digital Integrated Circuit,Microprocessors and Microcontroller,Digital Logic Design,Linar IC Applications,Electronic Devices and Circuits
- **Core CS**: Data Structures & Algorithms, OOP, Computer Networks
- **AI/ML**: Deep Learning, Machine Learning, Robotics

Achievements

•1591 Rating, Codechef Jan,2025

•Top 1.3%, JEE MAIN 2021 Feb,2021

•Hacktoberfest 2022, Pulled 4+3(extra) pull requests out of 4. Oct,2022

•DotSlash 6.0, Paricipated in **DotSlash 6.0,an 36 hours long Hackathon** and developed **FitCity.** Feb,2023